IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Previously presented) A semiconductor device assembly, comprising:
at least one semiconductor device; and
at least one resiliently compressible spacer protruding from a surface of the at least one semiconductor device, the at least one resiliently compressible spacer defining a distance the surface of the at least one semiconductor device is to be spaced apart from another semiconductor device to be positioned in superimposed relation with the at least one semiconductor device.

2. (Canceled)

3. (Previously presented) The semiconductor device assembly of claim 1, wherein the at least one resiliently compressible spacer protrudes from an active surface of the at least one semiconductor device.

4. (Canceled)

5. (Previously presented) The semiconductor device assembly of claim 4, comprising a plurality of spacers that are arranged to stably support the another semiconductor device.

6. (Previously presented) The semiconductor device assembly of claim 1, further comprising:
the another semiconductor device positioned adjacent the at least one resiliently compressible spacer, opposite from the at least one semiconductor device.

7. (Previously presented) The semiconductor device assembly of claim 6, further comprising:
adhesive material between the at least one semiconductor device and the another semiconductor device.

8. (Previously presented) The semiconductor device assembly of claim 7, wherein the adhesive material is located between adjacent spacers.

9. (Withdrawn and previously presented) The semiconductor device assembly of claim 6, wherein the at least one resiliently compressible spacer is electrically isolated from internal circuitry of the at least one semiconductor device.

10. (Previously presented) The semiconductor device assembly of claim 1, wherein the at least one resiliently compressible spacer comprises electrically conductive material.

11. (Previously presented) The semiconductor device assembly of claim 10, wherein the at least one resiliently compressible spacer communicates with a ground plane of the at least one semiconductor device.

12. (Original) The semiconductor device assembly of claim 1, further comprising:
a substrate with which at least one semiconductor device is associated.

13. (Previously presented) The semiconductor device assembly of claim 12, wherein the substrate comprises at least one of a circuit board, an interposer, a semiconductor device, and leads.

14. (Previously presented) The semiconductor device assembly of claim 12, wherein at least one bond pad of the at least one semiconductor device is in communication with a corresponding contact area of the substrate.

15. (Previously presented) The semiconductor device assembly of claim 14, further comprising:

at least one discrete conductive element extending from the at least one bond pad, over an active surface of the at least one semiconductor device, to the corresponding contact area.

16. (Previously presented) The semiconductor device assembly of claim 15, wherein heights of the at least one resiliently compressible spacer exceeds a maximum height the at least one discrete conductive element protrudes above the active surface.

17. (Previously presented) The semiconductor device assembly of claim 1, wherein the at least one resiliently compressible spacer is secured to noncircuit bond pads of the at least one semiconductor device.

18. (Previously presented) A semiconductor device assembly, comprising:

a substrate;

a first semiconductor device associated with the substrate, bond pads of the first semiconductor device in communication with corresponding contact areas of the substrate;

mutually laterally spaced discrete spacers positioned on and protruding from an active surface of the first semiconductor device, at least one spacer of the mutually laterally discrete spacers being in communication with a ground or reference voltage plane of the first semiconductor device; and

a second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers, the at least one spacer establishing communication between the back side of the second semiconductor device and the ground or reference voltage plane.

19. (Previously presented) The semiconductor device assembly of claim 18, wherein the substrate comprises one of a circuit board, an interposer, another semiconductor device, and leads.

20. (Previously presented) The semiconductor device assembly of claim 18, wherein the bond pads and the corresponding contact areas communicate by way of discrete conductive elements positioned therebetween.

21. (Previously presented) The semiconductor device assembly of claim 20, wherein the discrete conductive elements comprise at least one of bond wires, tape-automated bond elements, and thermocompression bonded leads.

22. (Previously presented) The semiconductor device of claim 18, wherein the mutually laterally spaced discrete spacers are secured to noncircuit bond pads of the first semiconductor device.

23. (Previously presented) The semiconductor device assembly of claim 22, wherein the mutually laterally spaced discrete spacers comprise conductive material.

24. (Withdrawn and previously presented) The semiconductor device assembly of claim 23, wherein the mutually laterally spaced discrete spacers are electrically isolated from internal circuitry of the first semiconductor device.

25. (Previously presented) The semiconductor device assembly of claim 23, wherein the mutually laterally spaced discrete spacers are in communication with a ground or reference voltage plane of the first semiconductor device.

26. (Canceled)

27. (Canceled)

28. (Previously presented) The semiconductor device assembly of claim 18, wherein at least one of the mutually laterally spaced discrete spacers is compressible.

29. (Withdrawn and previously presented) The semiconductor device assembly of claim 18, wherein the second semiconductor device comprises a dielectric layer on at least portions thereof that contact the mutually laterally spaced discrete spacers.

30. (Previously presented) The semiconductor device assembly of claim 18, wherein bond pads of the second semiconductor device communicate with the corresponding contact areas of the substrate by way of discrete conductive elements positioned therebetween.

31. (Previously presented) The semiconductor device assembly of claim 18, further comprising:
an adhesive layer between the first semiconductor device and the second semiconductor device.

32. (Previously presented) The semiconductor device assembly of claim 31, wherein at least some of the mutually laterally spaced discrete spacers extend through the adhesive layer.

33. (Previously presented) The semiconductor device assembly of claim 18, further comprising:
at least one additional semiconductor device positioned over the second semiconductor device.

34. (Previously presented) The semiconductor device assembly of claim 18, further comprising:
an encapsulant material substantially covering the first semiconductor device, the second semiconductor device, discrete conductive elements, and portions of the substrate located adjacent to the first semiconductor device.

35. (Previously presented) The semiconductor device assembly of claim 18, further comprising:

at least one external connective element carried by the substrate and in electrical communication with at least one corresponding contact area of the substrate.

36-52. (Canceled)

53. (Previously presented) The semiconductor device assembly of claim 1, wherein the at least one resiliently compressible spacer is secured to a contact pad of the at least one semiconductor device.

54. (Previously presented) The semiconductor device assembly of claim 18, wherein the at least one spacer is secured to a contact pad of at least one of the first semiconductor device and the second semiconductor device.